This listing of claims replaces all prior listings of the claims in the application.

In the Claims:

1. (canceled)

2. (currently amended) The method of Claim ~~1~~ 25 wherein said integrated circuit memory is of the type selected from dynamic random access memory DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory.

3. (currently amended) The method of Claim ~~1~~ 25 wherein said failed memory element is replaced with a redundancy element selected from the group consisting of at least row redundancy element and column redundancy element.

4. (currently amended) The method of Claim ~~1~~ 25 wherein said failed memory element is replaced with a redundancy element by electrically alterable circuit connections.

5. (currently amended) The method of Claim 4 wherein said electrically alterable circuit connections include at least one connection element selected from the group consisting of electronic fuse and electronic anti-fuse.

6-7. (canceled)

8. (currently amended) ~~The method of claim 1~~ A method for identifying a failed memory element within an integrated circuit memory and for repairing said integrated circuit memory, comprising:

providing an integrated circuit memory having a plurality of banks,

storing data bits and error correction code ("ECC") check bits to individual

locations of said integrated circuit memory;

thereafter retrieving data bits and ECC check bits from said individual locations;

recording at least single-bit failure locations in said integrated circuit memory based on processing said retrieved data bits together with said retrieved ECC check bits;

based on said recorded failure locations, using first logic circuits within said integrated circuit to automatically identify a failed memory element in one bank of said plurality of banks; and

using at least second logic circuits within said integrated circuit to automatically replace said failed memory element in said one bank with a redundancy element,

wherein said failure locations are automatically identified and recorded while said integrated circuit is in a normal operational mode and wherein said failed memory element is automatically replaced only during a non-normal operational mode of said integrated circuit.

9. (currently amended) The method of Claim 8 wherein said non-normal operational mode ~~is of~~ has a type selected from power-up mode or power-down mode.

10. (canceled)

11. (currently amended) The method of Claim ~~10~~ 25 wherein said integrated circuit memory is of the DRAM type and wherein said locations are automatically identified and recorded while said integrated circuit is in a normal operational mode.

12. (original) The method of Claim 11 wherein said failed memory element is automatically replaced when said integrated circuit remains installed within a product for normal use.

13. (canceled)

14. (currently amended) The integrated circuit of Claim ~~13~~ 26 wherein said memory is of the type selected from dynamic random access memory (DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory.

15. (currently amended) The integrated circuit of Claim ~~13~~ 26 wherein said means for automatically replacing a failed memory element includes electrically alterable circuit connections.

16. (currently amended) The integrated circuit of Claim 15 wherein said electrically alterable circuit connections include at least one connection selected from electronic fuse and electronic anti-fuse.

17. (currently amended) The integrated circuit of Claim ~~13~~ 26 wherein said ~~register, said means for identifying and said means for replacing all operate~~ failed memory element is identified and replaced while said integrated circuit is in a normal operational mode.

18-19. (canceled)

20. (currently amended) The integrated circuit of Claim ~~19~~ 26 wherein said non-normal operational mode is of a type selected from power-up mode or power-down mode.

21. (currently amended) The integrated circuit of Claim ~~14~~ 26 wherein said integrated circuit includes a microprocessor.

22. (currently amended) The integrated circuit of Claim ~~21~~ 20 wherein said memory is of the DRAM type and wherein ~~said register records~~ said locations of said

failures are recorded while said integrated circuit is in a normal operational mode.

23. (currently amended) The integrated circuit of Claim ~~22~~ 26 wherein said means for automatically replacing said failed memory element operates when said integrated circuit remains installed within a product for normal use.

24. (currently amended) The integrated circuit of Claim ~~13~~ 26 wherein said redundancy element is selected from the group consisting of at least row redundancy element and column redundancy element.

25. (new) A method for identifying a failed memory element within an integrated circuit memory and for repairing said integrated circuit memory, comprising:

providing an integrated circuit memory having a plurality of banks;

automatically identifying and recording locations of failures within said integrated circuit memory by storing data bits and error correction code ("ECC") check bits to individual locations of said integrated circuit memory;

thereafter retrieving data bits and ECC check bits from said individual locations;

recording at least single-bit failure locations in said integrated circuit memory based on ECC processing said retrieved data bits together with said retrieved ECC check bits;

based on said recorded failure locations, using first logic circuits within said integrated circuit to automatically identify a failed memory element in one bank of said plurality of banks; and

asserting a busy signal for said one bank while servicing memory access requests by banks of said plurality of banks other than said one bank and while using at least second logic circuits within said integrated circuit to automatically replace said

failed memory element in said one bank with a redundancy element.

26. (new) An integrated circuit including a self-repairing memory having a plurality of banks, comprising:

a memory;

error correction code (ECC) logic circuits coupled to said memory, said ECC logic circuits operable to detect errors within strings of data bits and check bits retrieved from addressed storage locations within said memory;

means for recording locations of at least single-bit failures from said detected errors;

means for automatically identifying a failed memory element in one of said plurality of banks based on said recorded locations;

means for asserting a busy signal for said one bank;

means for automatically replacing said failed memory element in said one bank with a redundancy element; and

means for providing access to banks of said plurality of banks other than said one bank while said failed memory element is identified and replaced.

27. (new) The method of Claim 8 wherein said integrated circuit memory is of the type selected from dynamic random access memory DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory.